Abstract

An apparatus for link layer port-based hardware implemented acceptance rate limiting control is presented. The apparatus employs a single up-down counter tracking a receive port buffer occupancy level. The single up-down counter is incremented by a receive line rate clock signal time truncated by a frame receive signal and a feedback frame acceptance control signal. The single up-down counter is decremented at an Service Level Agreement (SLA) agreed upon committed rate at which content is extracted from the receive port buffer. Outputs of comparators determining when the port receive buffer occupancy level is below a low watermark receive port buffer occupancy level, and when the receive port buffer occupancy level is above a maximum burst size, are provided to a master slave flip flop generating the frame acceptance control signal exhibiting hysteresis as the port receive buffer occupancy level transitions between the low watermark and the maximum burst size receive port buffer occupancy levels. The advantages of the link layer port-based hardware implemented acceptance rate limiting control achieved are derived from a deterministic response enforced in real time, at line rate, as content is being received employing a small number of logic gates.